

# Detector Support Group Select Projects

Amrit Yegneswaran

# DSG Staff



Mary Ann (20)



Peter (27)



Aaron (<1)



Pablo (4)



Brian (20)



George (5)



Mindy (20)



Tyler (4)

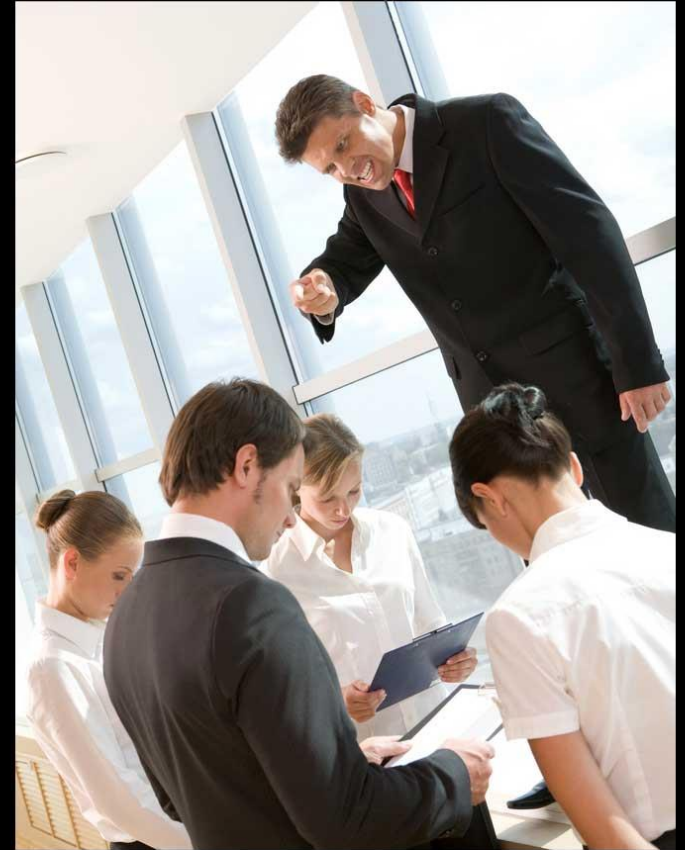


Marc (23)

*Give me the child for the first **seven** years and I will **give** you the **man**.*  
Jesuit maxim widely attributed to Ignatius Loyola

**DSG is all about teamwork**

(c) Teamwork-Quotes.com



**T-E-A-M-W-O-R-K**

Teamwork is a lot of people  
doing what **I** say.

# Contents



- **Hall A**

- SBS & BB: cable fabrication; super-module fabrication; GEM gas system
- HRS: dipole magnet power supply's controls and monitoring system

- **Hall B**

- RICH: cooling; humidity and temperature sensor
- Torus & Solenoid: readout system

- **Hall C**

- HMS/SHMS: magnet HMI screens → CSS-BOY; HV Tcl/Tk screens → CSS-BOY
- NPS: testing of CAEN SY4527

- **Hall D**

- Solenoid: upgrade of PXI system; WEDM screens

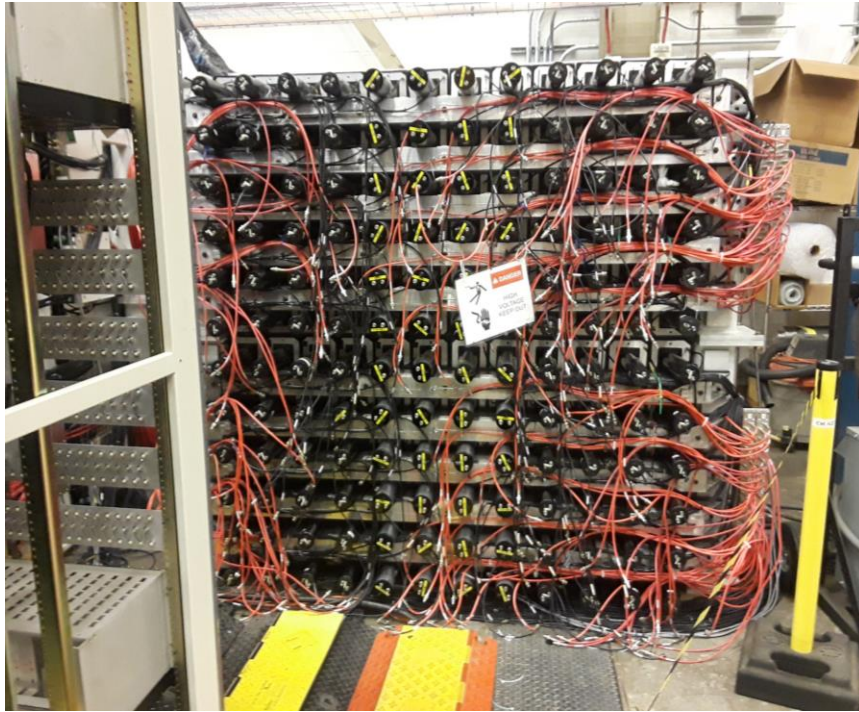
- **DSG**

- Accelerator: populating VME fast shutdown board, wire-bonding tests
- R&D & Safety: Test stations; focus on safety



# Hall A: SBS Cable Fabrication and Routing

- Cable fabrication for HCAL
  - Search, seize, and secure cables in ESB
  - 95% of ~1888 cables fabricated
- HCAL HV cable labeling and routing



~300 HV cables routed on HCAL in Test Lab

[DSG Note 2019-45](#)



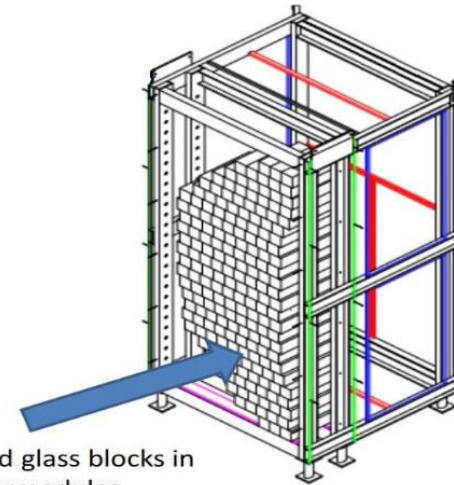
Search, seize, and secure cables in ESB

“He believed in youth and youth made him its confidant”  
dedication to George Edward Cunningham, Berkeley CA



# Hall A: BB ECAL Super-module Assembly

- 126/191 super-modules assembled.



1719 lead glass blocks in 191 supermodules

- Each super-module has:
  - Nine lead-glass blocks with light guides
  - Wrapped in aluminum foil and copper
  - Support frame with screws, springs, and plates hold them in place



Top: diagram of BigBite ECAL showing configuration of 191 super-modules

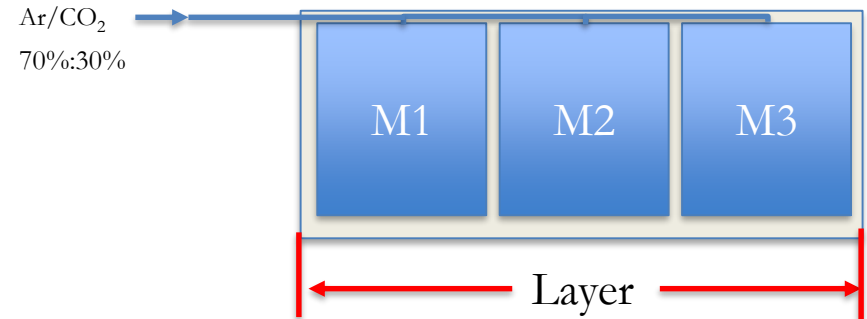
Left: Partially assembled super-module showing the nine wrapped lead-glass blocks. Light guides are on opposite end of blocks in photo

[DSG Note 2019-48](#)

# Hall A: SBS & BB GEM Gas System

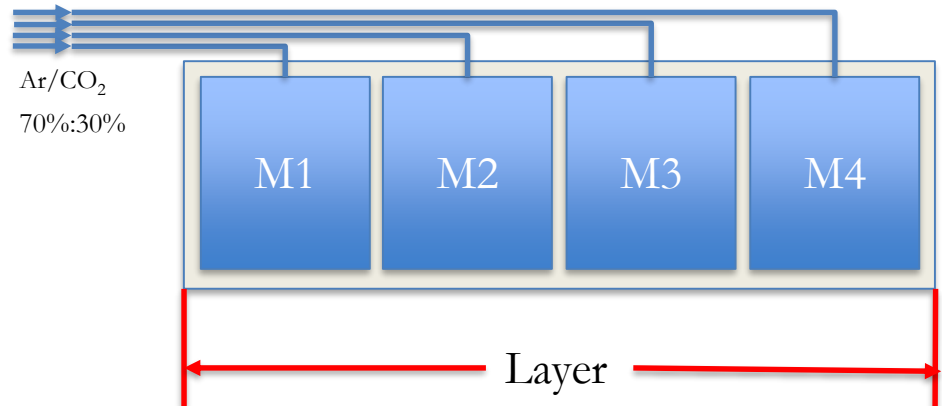
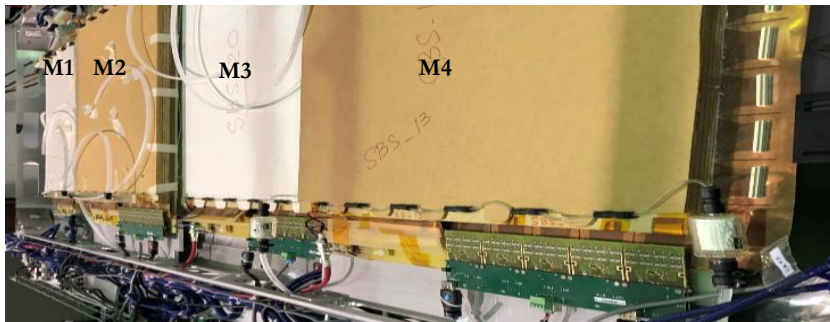
## INFN Layer Configuration

3 modules per layer  
1 gas line per layer



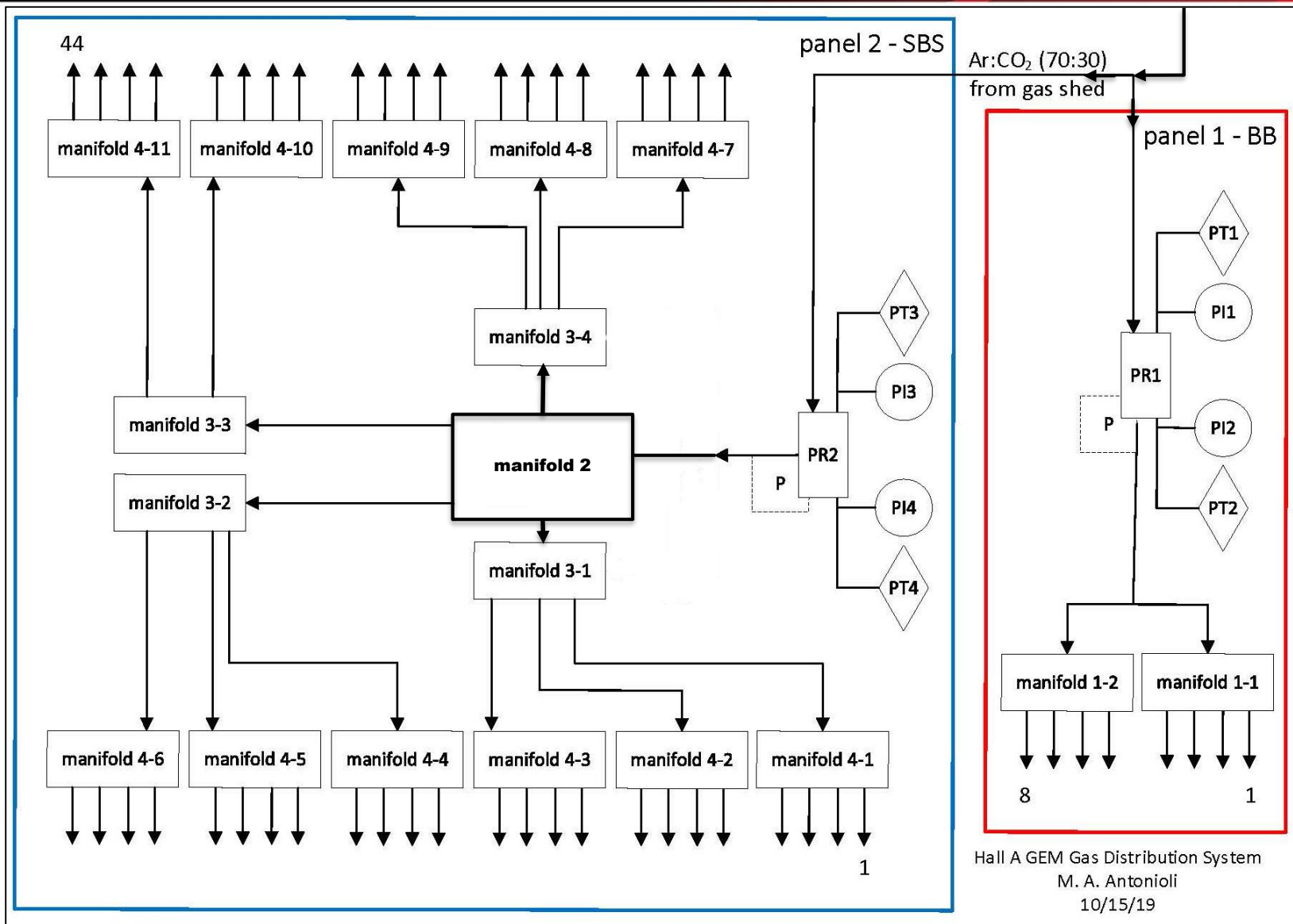
## UVA Layer Configuration

4 Modules per layer  
4 Gas line Per layer



[DSG Talk 2019-17](#)

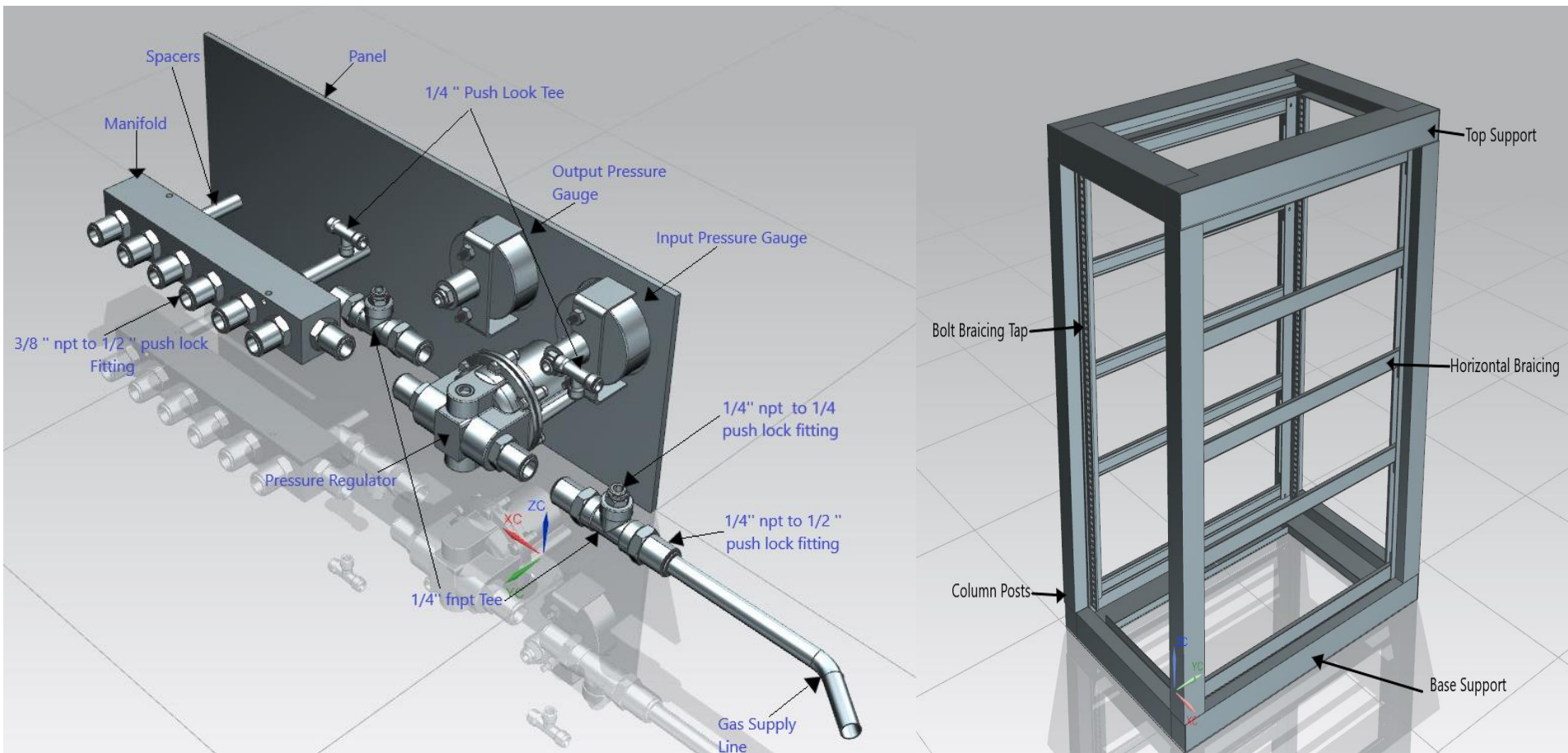
# Hall A: SBS & BB GEM Gas System





# Hall A: SBS & BB GEM Gas System

- Developing 3D-CAD model of gas system in NX-12



Isometric View of GEM Gas System's components

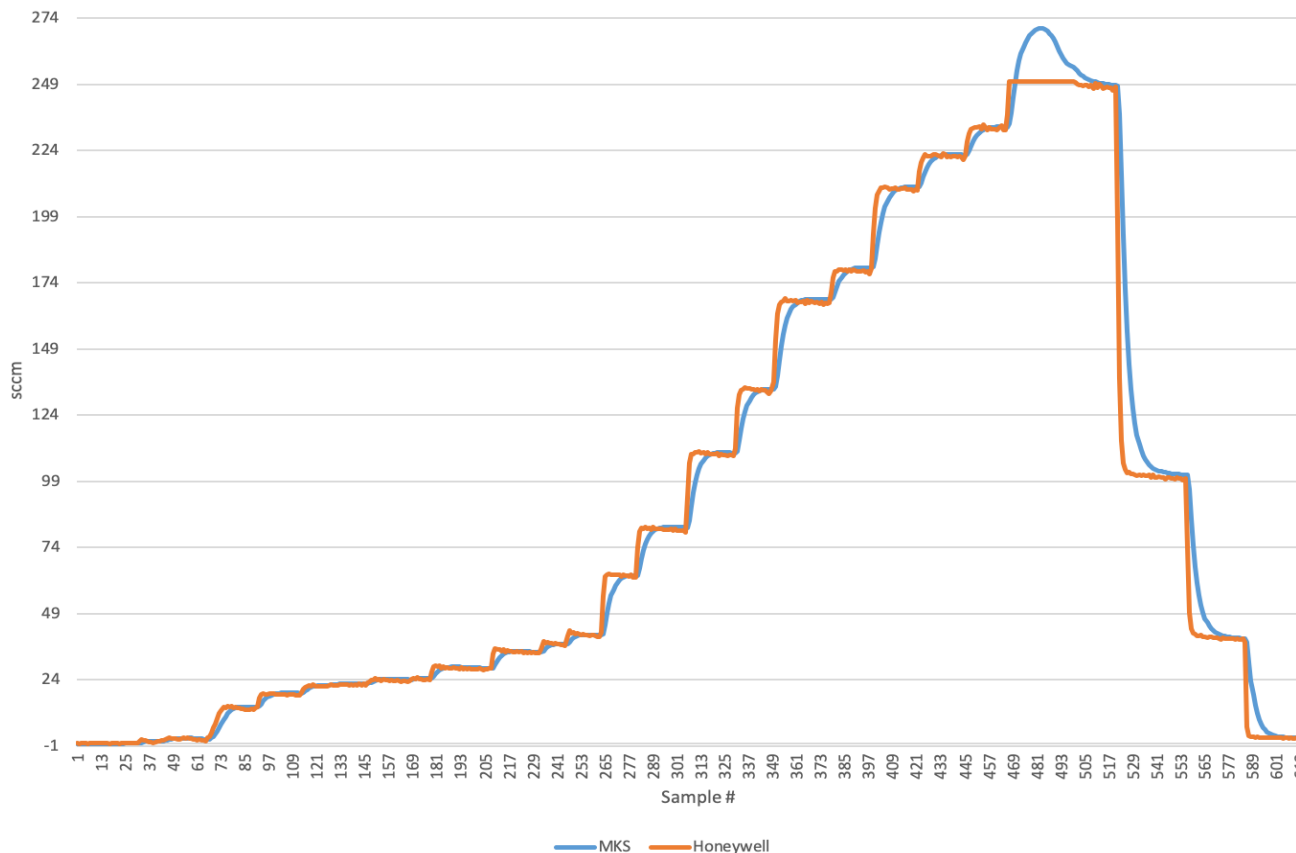
Isometric View of GEM Gas System's rack assembled



# Hall A: SBS & BB GEM Gas System

- Honeywell Zephyr Evaluation

MKS GE50 vs Honeywell Zephyr Flow Sensors @ 4 Hz



<b>Series</b>	<b>Honeywell Zephyr™ HAF Series-High Accuracy ±50 SCCM to ±750 SCCM</b>
<b>Signal conditioning</b>	amplified, compensated
<b>Technology</b>	silicon die with thermally isolated heater
<b>Flow/pressure range</b>	±50 SCCM to ±750 SCCM
<b>Output</b>	analog (Vdc), digital (I <sup>2</sup> C)
<b>Power consumption</b>	<b>3.3 Vdc:</b> 40 mW typ. (no load) (analog); 23 mW typ. (no load) (digital) <b>5.0 Vdc:</b> 55 mW typ. (no load) (analog); 38 mW typ. (no load) (digital)
<b>Port style</b>	long port, short port
<b>Media compatibility</b>	dry non-corrosive gases
<b>Temperature range</b>	<b>operating:</b> -20°C to 70°C [-4°F to 158°F] <b>compensated:</b> 0°C to 50°C [32°F to 122°F]
<b>Dimensions (H x W x D)</b>	<b>long port:</b> 20 mm x 36 mm x 19.9 mm [0.79 in x 1.42 in x 0.78 in]; <b>short port:</b> 17.6 mm x 28.8 mm x 19.9 mm [0.69 in x 1.13 in x 0.78 in]
<b>Features</b>	high accuracy, high sensitivity at very low flows, high stability, low pressure, linear output, customizable, full calibration and temperature compensation

[DSG Talk 2019-17](#), [DSG Note 2019-49](#), [DSG Note 2019-50](#)

# Hall A: Dynapower PLC Control System

- Upgrade of PLC used in HRS Dipole Magnet Power Supplies
  - Evaluated potential systems (different vendors & products)
  - Setup (code development) and deployed selected system



OLD – SLC500



NEW - CompactLogix

[DSG-Note 2019-29](#), [DSG-Note 2019-40](#)

# Thanks Jack

Dsg-halla <dsg-halla-bounces@jlab.org>  
on behalf of Jack Segal <segal@jlab.org>  
Tue 6/11/2019 8:34 PM

Brian,

Many thanks to you and the DSG. The Left Dipole finally seems to be doing what it was intended to do 24 years ago. It now has redundant protections that function correctly. Your prompt help while I was trying to understand how things were configured and how to correct the errors is much appreciated. Again, thanks!



DSG's inner child



# Hall B: RICH Cooling Investigation

Electronic Panel

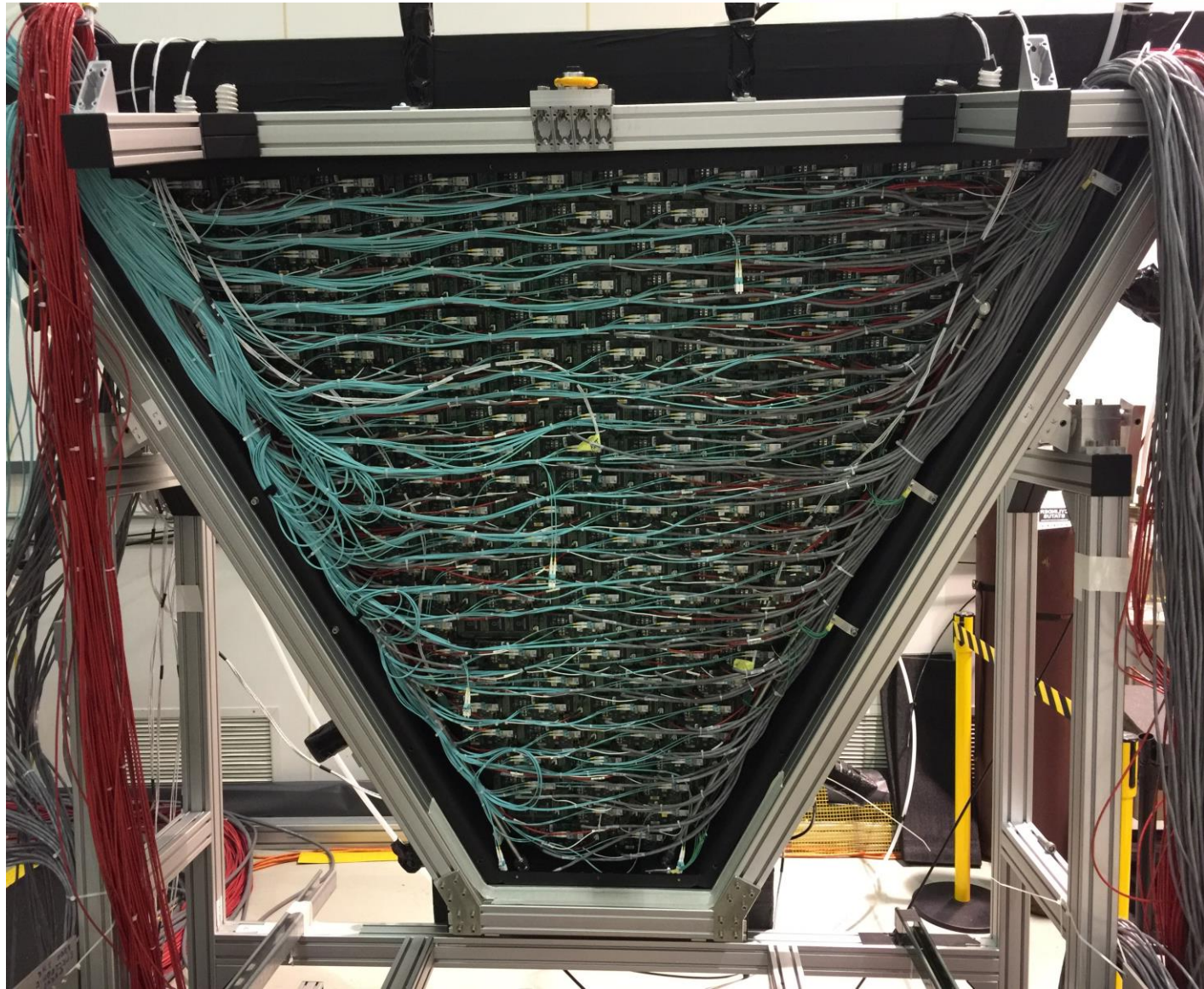
Internal cabling

Red ~ HV

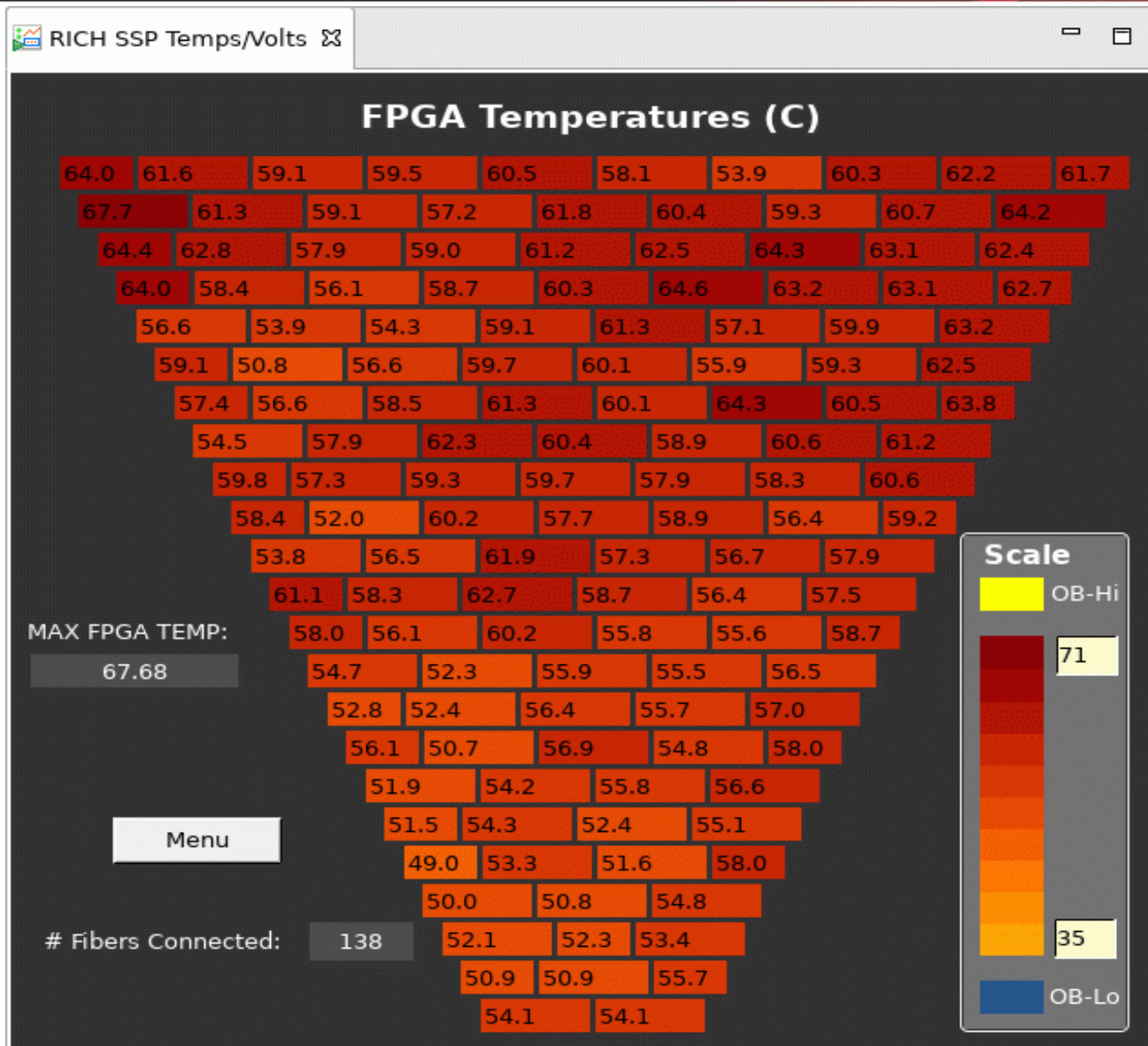
Gray ~ LV

Light gray ~ Sensor

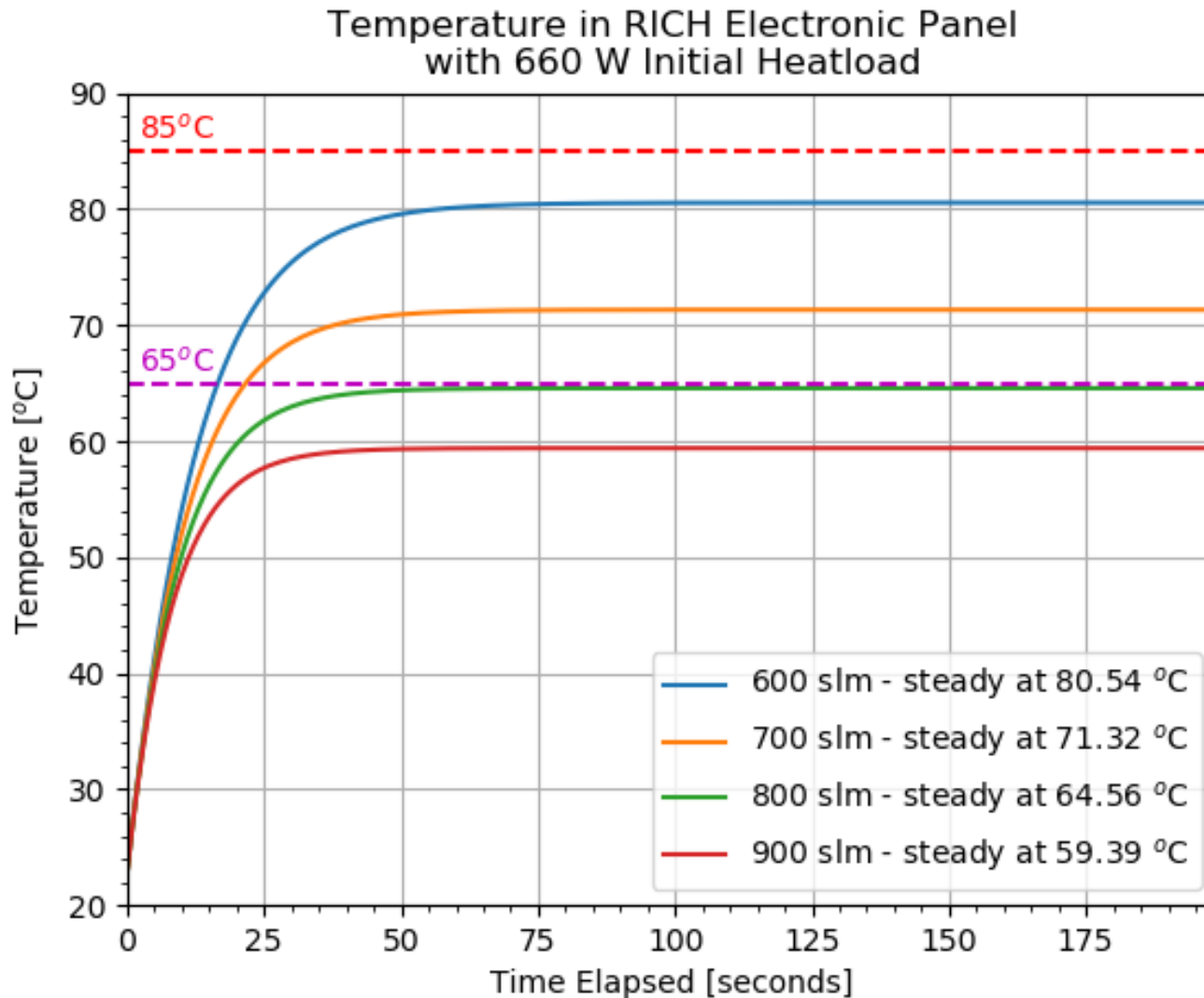
Green ~ Data



# Hall B: RICH Cooling Investigation



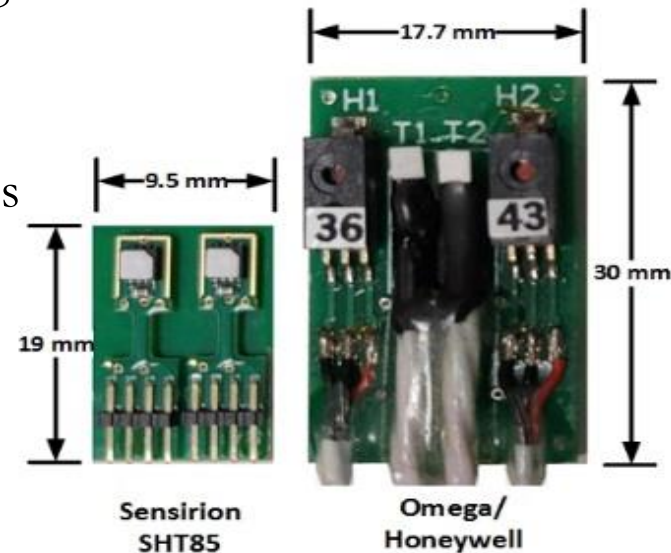
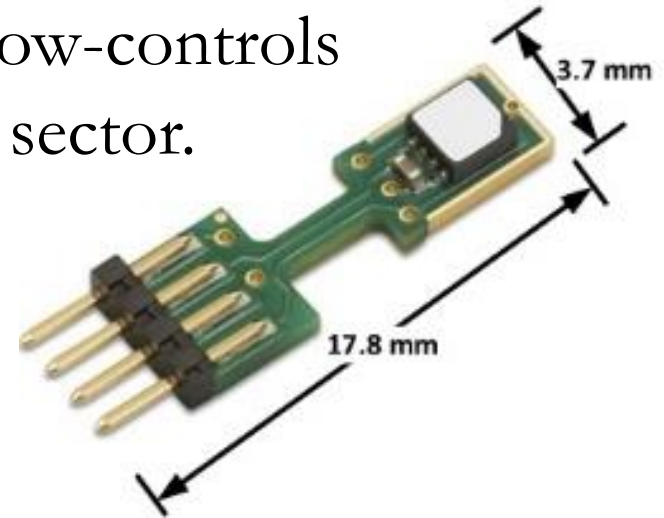
# Hall B: RICH Cooling Investigation





# Hall B: Sensors for New RICH

- Improve temperature and humidity slow-controls measurement systems for next RICH sector.
- Sensirion SHT85 Sensor
  - New product released on 11/2018
  - Accuracy
    - ✓ Humidity:  $\pm 1.5\%$  RH, temperature:  $\pm 0.1^\circ\text{C}$
- Compare to currently used Honeywell/Omega
  - Smaller size of sensor assembly
  - Reduced # of cables/connectors
  - Compatible with existing slow-controls electronics
  - Compatible software support (including EPICS)
  - Lower cost



# HallB: Sensors for New RICH

- Developing FPGA code
  - Addressed issue with single-shot readout sequence
  - Testing in progress

[DSG Note 2019-44](#)

[DSG Note 2019-47](#)

Sensirion SHT85 - Development - Periodic DAQ Readout (fetch) Sequence - V3.vi Front Panel on I2C.lvproj/FPGA Target \*

File Edit View Project Operate Tools Window Help

17pt Application Font

Select Sensor - SCL/SDA SCL/SDA1

Start Stop

ST Initialize 0 0  
ST Init Hold 2 2  
ST SCL High 2 2  
ST SDA Low 0 0  
ST SCL Low 0 0  
ST End Hold 4 4

Addr W & R Byte

Wbyte SCL High 2  
W byte SCL Low 2  
Wbyte SDA 2  
Wbyte SDA - SCL Delay 0

Master ACK Control

SCL High (uSec) 2  
SCL Low (uSec) 2  
SDA (uSec) 2

Command Byte Control

Cmd SCL High 2  
Cmd SDA 2  
Cmd SCL Low 2

Read Byte Control

SCL High (uSec) 2  
SDA (uSec) 0  
SCL Low (uSec) 4

Read ACK Control

Init Wait 2 0  
Pre SCL Low 2 Disabled  
SCL Low 2 2 SCL High 2  
Pre SDA Low 2 Enabled 1 Pre SDA Low 3  
Pre OE Wait 2 2  
Pre Clk OE 2 Set High 0 OE lenght 2  
Post OE Wait 2 0  
Post SCL ACK Wait 2 0  
Post Clk OE 1 En 2 Enabled Post Clk OE 3 Set Low  
ACK Wait Loop 2 Enabled  
Post ACK Wait 2 4  
Post Clk OE 2 En 2 Disabled Post Clk OE 4 Set Low

Read Sequence Loop Control

stop Loop Delay(mSec) 500  
STOP  
Read Loop Count 27

Sensor Ack Read Ack Type

Master OE Enable off Low Master OE Level  
Master Out Data Ena off Low Master Data Level

NACK High ACK Low

T MSB Byte d100 H MSB Byte d46  
T LSB Byte d147 H LSB Byte d134  
T CRC Bvte d61 H CRC Byte d236

Temp Dec Raw F d25747 74.7553 (F) Temp OK Temp CRC Error  
H Dec Raw F d11910 18.1735 (%) Humidity OK H CRC Error

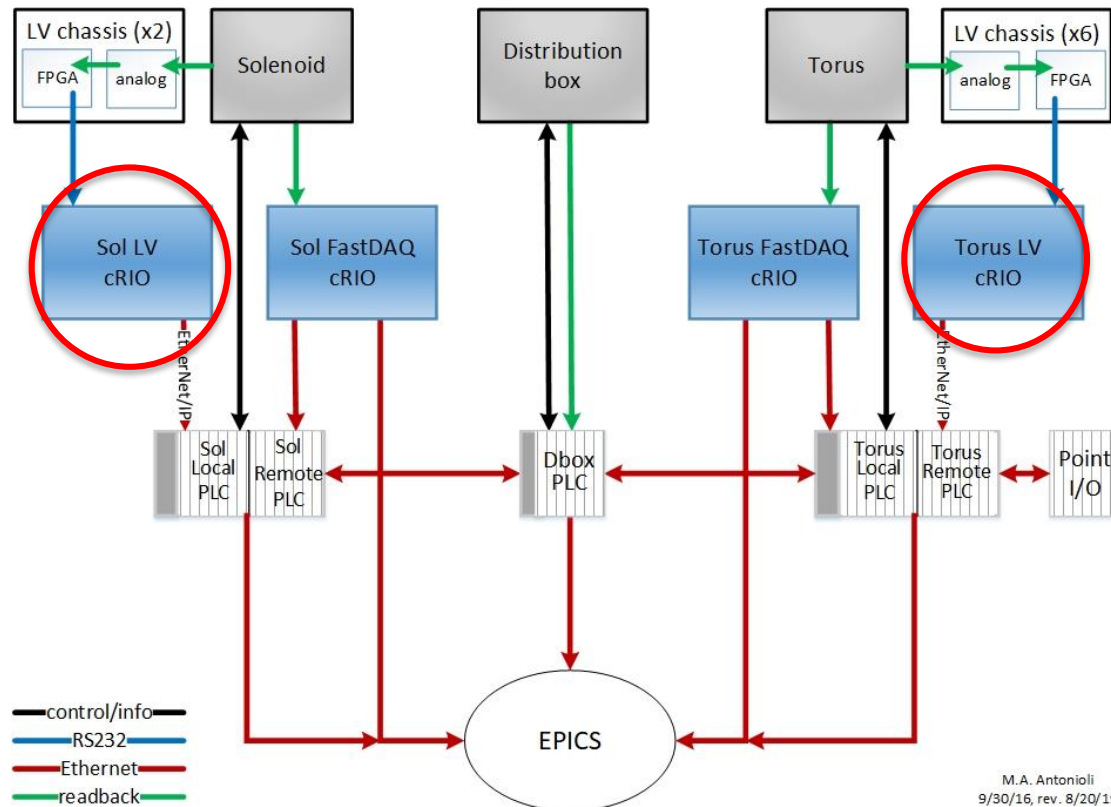
Check CRC ON

I2C.lvproj/FPGA Target

Serial Communication Timing Test Screen

# Hall B: Solenoid and Torus Magnet Readout System

- Replace current LV Chassis FPGA with DE0-Nano-SoC or some other improved FPGA board
  - LV cRIOs have failed, removing them eliminates point of failure
  - New board would communicate directly with PLC



Present readout configuration

M.A. Antonilli  
9/30/16, rev. 8/20/19



# Thanks Ruben

Dsg-hallb\_magnets  
on behalf of Ruben Fair  
Thu 9/5/2019 10:11 AM

Tyler and the DSG,  
This is excellent work. Great report and summaries.

We very much appreciate your contribution and your continuous improvement efforts. Looking forward to seeing which solution is the most reliable and cost effective.

Thank you  
Ruben



DSG's inner child

- Motivation
  - Standardization
  - Enables data archiving and thereby facilitates debugging
  - Enhancements of display and functions facilitates magnets' controls and monitoring
- 275 HMI screens need to be addressed

[DSG Note 2019-20](#)

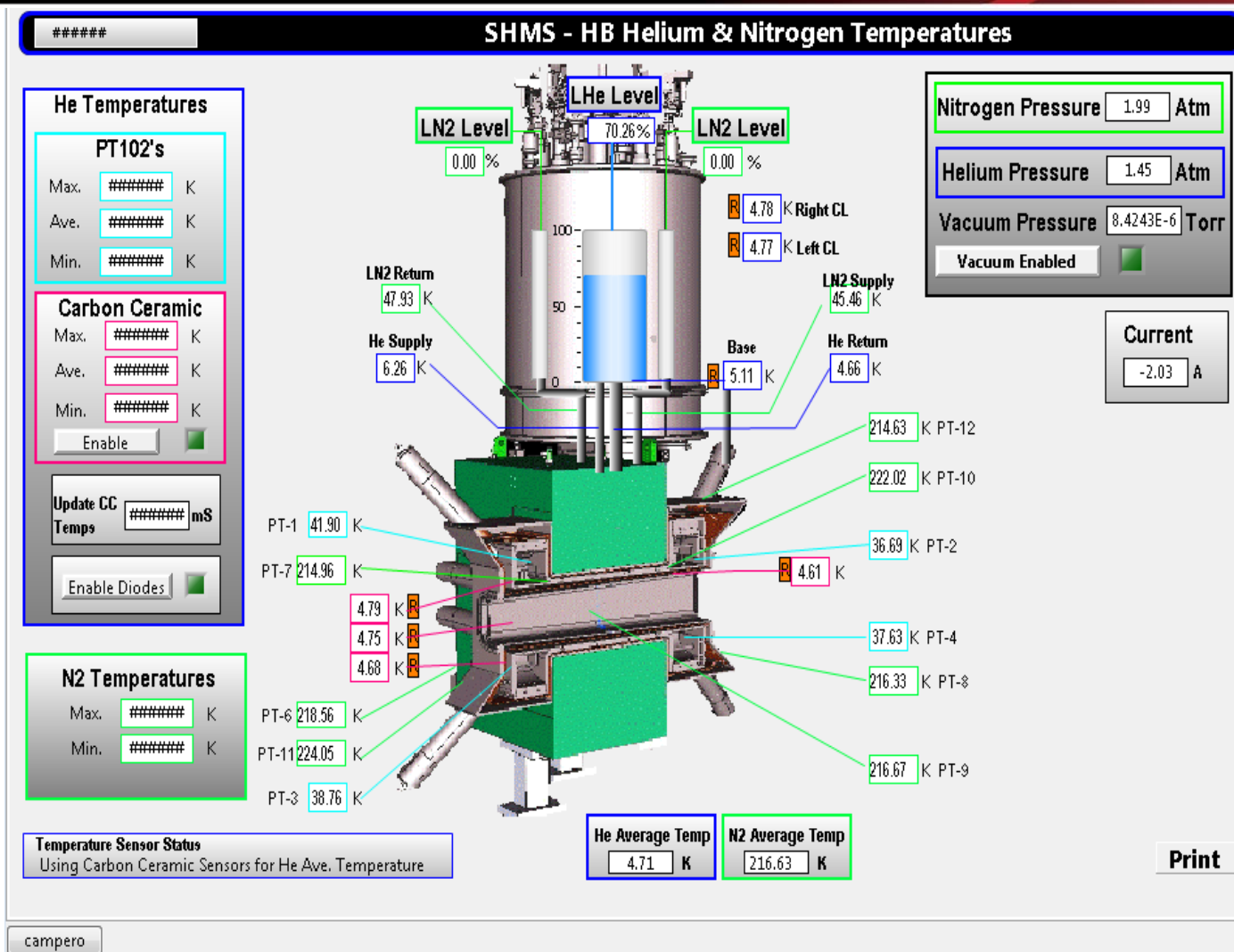
[DSG Note 2019-22](#)

[DSG Note 2020-02](#)

[DSG Talk 2019-07](#)

[DSG Talk 2019-13](#)

# Hall C: HMS/SHMS Magnet HMI screens to EPICS CSS-BOY



CSS-BOY screen for SHMS – Horizontal Bender magnet’s Helium and Nitrogen temperatures. This screen combines Helium and Nitrogen HMI PLC screens.



# Hall C: HV Tcl/Tk system to EPICS CSS-BOY

- Motivation for CSS
  - Standardization
  - Faster
    - ✓ Opens screens in seconds as opposed to minutes (yawn)
    - ✓ Screens are static and do not have to be rebuilt unless configurations change
  - Uses a Python script to build screens based on configuration files.
    - ✓ Script builds all screens in seconds
  - Includes CSS-compatible backup/restore program and start-up script.
  - Start-up script allows multiple instances of screens to be opened simultaneously and provides a consistent user experience for all users

[DSG Note 2019-27](#), [DSG Note 2019-34](#), [DSG Note 2019-36](#), [DSG Note 2019-42](#)

[DSG Talk 2019-13](#)

# Hall C: HV Tcl/Tk system to EPICS CSS-BOY

**HMS Hodo 1 Y HV Controls** Group ▾

Ch ID	On/Off	Status	Vmon	Imon	Vset	Itrip	Vmax	RmpUp	RmpDwn
h1y01+	OFF	OFF	0.0	0	1675.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y02+	OFF	OFF	0.0	0	1810.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y03+	OFF	OFF	0.4	3	1865.0 V	2700.0 uA	1900.0 V	100.0 V/s	100.0 V/s
h1y04+	OFF	OFF	0.0	0	1848.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y05+	OFF	OFF	0.0	0	1835.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y06+	OFF	OFF	0.0	0	1829.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y07+	OFF	OFF	0.0	0	1825.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y08+	OFF	OFF	0.0	0	1827.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y09+	OFF	OFF	0.0	0	1920.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y10+	OFF	OFF	1.0	1	1785.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y01-	OFF	OFF	0.0	0	1760.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y02-	OFF	OFF	0.0	0	1815.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y03-	OFF	OFF	0.0	0	1920.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y04-	OFF	OFF	0.0	1	1760.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y05-	OFF	OFF	0.0	0	1790.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y06-	OFF	OFF	0.0	0	1840.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y07-	OFF	OFF	0.0	0	1815.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y08-	OFF	OFF	0.0	0	1830.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y09-	OFF	OFF	0.0	0	1860.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
h1y10-	OFF	OFF	0.0	0	1800.0 V	1000.0 uA	1950.0 V	500.0 V/s	500.0 V/s
ALL CHANNELS	OFF					Itrip	Vmax	RmpUp	RmpDwn
	ON					0.0	0.0	0.0	0.0

List-view controls screen for HMS Hodoscope 1 Y.

# Hall C: Investigation of CAEN SYS 4527 and HV cards A7030TN

- Issues with SY4527 and HV card A7030TN
  - Changing set values of parameters
  - Ramp-up latency
  - Ignoring commands

[DSG Note 2019-46](#)

[DSG Note 2019-54](#)

[DSG Note 2020-01](#)

[DSG Talk 2019-18](#)

[DSG Talk 2019-23](#)

[DSG Talk 2019-28](#)

TEST HV CAEN - Expert Controls - Slot 1

Novice
Board Model: A7030TN - [S/N: 297]
ALL ON/OFF

Ch#	Location	Click to Turn	Status	VMon [V]	Imon [uA]	Vset [V]		Iset [uA]		Vmax [V]		RUp [V/s]		RDwn [V/s]		Trip [s]	
						Readback	Set	Readback	Set	Readback	Set	Readback	Set	Readback	Set	Readback	Set
00	DSG-Lab	OFF	ON	1499.73	-0.016	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
01	DSG-Lab	OFF	ON	1499.88	0.006	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
02	DSG-Lab	OFF	ON	1499.89	-0.104	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
03	DSG-Lab	OFF	ON	1499.83	-0.042	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
04	DSG-Lab	OFF	ON	1499.75	-0.078	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
05	DSG-Lab	OFF	ON	1499.94	-0.032	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
06	DSG-Lab	OFF	ON	1499.85	2.976	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
07	DSG-Lab	OFF	ON	1499.89	-0.118	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
08	DSG-Lab	OFF	ON	1499.82	-0.034	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
09	DSG-Lab	OFF	ON	1499.89	-0.036	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
10	DSG-Lab	OFF	ON	1499.75	0.922	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
11	DSG-Lab	OFF	ON	1499.86	-0.028	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
12	DSG-Lab	OFF	ON	1499.86	-0.070	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
13	DSG-Lab	OFF	ON	1499.79	-0.124	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
14	DSG-Lab	OFF	ON	1499.90	-0.020	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
15	DSG-Lab	OFF	ON	1500.04	-0.036	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
16	DSG-Lab	OFF	ON	1499.78	-0.042	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
17	DSG-Lab	OFF	ON	1499.75	-0.020	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
18	DSG-Lab	OFF	ON	1499.89	-0.062	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
19	DSG-Lab	OFF	ON	1499.87	0.038	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
20	DSG-Lab	OFF	ON	1499.96	-0.010	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
21	DSG-Lab	OFF	ON	1499.72	-0.004	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
22	DSG-Lab	OFF	ON	1499.90	-0.030	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
23	DSG-Lab	OFF	ON	1499.93	-0.068	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
24	DSG-Lab	OFF	ON	1499.99	-0.020	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
25	DSG-Lab	OFF	ON	1499.93	-0.018	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
26	DSG-Lab	OFF	ON	1499.80	0.002	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
27	DSG-Lab	OFF	ON	1499.78	0.030	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
28	DSG-Lab	OFF	ON	1499.95	-0.006	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
29	DSG-Lab	OFF	ON	1499.68	-0.032	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
30	DSG-Lab	OFF	ON	1499.91	-0.040	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
31	DSG-Lab	OFF	ON	1499.68	-0.076	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
32	DSG-Lab	OFF	ON	1499.82	-0.018	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
33	DSG-Lab	OFF	ON	1499.76	-0.042	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
34	DSG-Lab	OFF	ON	1499.84	-0.062	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0
35	DSG-Lab	OFF	ON	1499.80	-0.034	1500.00	1500	1000.00	1000.00	1800	1800	25	25	25	25	3.0	3.0

HV- CAEN MAIN

Max Current: Hwd 1108 microAm

Max Voltage: Hwd 3156 Volt

Board Temperature 25 Celsius

I & V Plots

Ramp Up Test

All Channels

VSet [V]	I Set [uA]	VMax [V]	Rup [V/s]	RDown[V/s]	Trip [s]
1500.0	1000.0	1800.0	25.0	25.0	3.0

Next Slot >

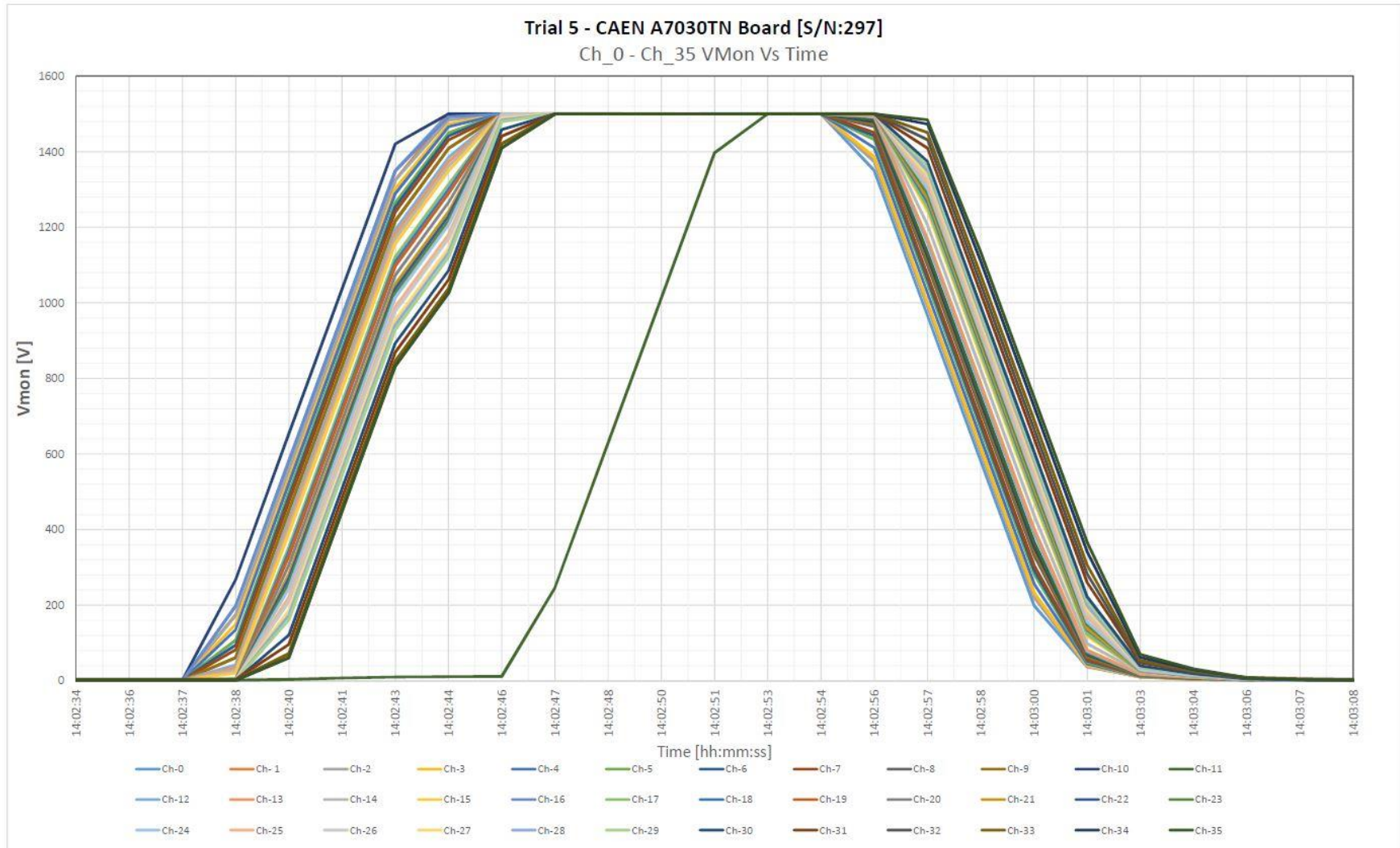
< Previous Slot

HV CAEN Expert Controls CSS-BOY screen developed for testing





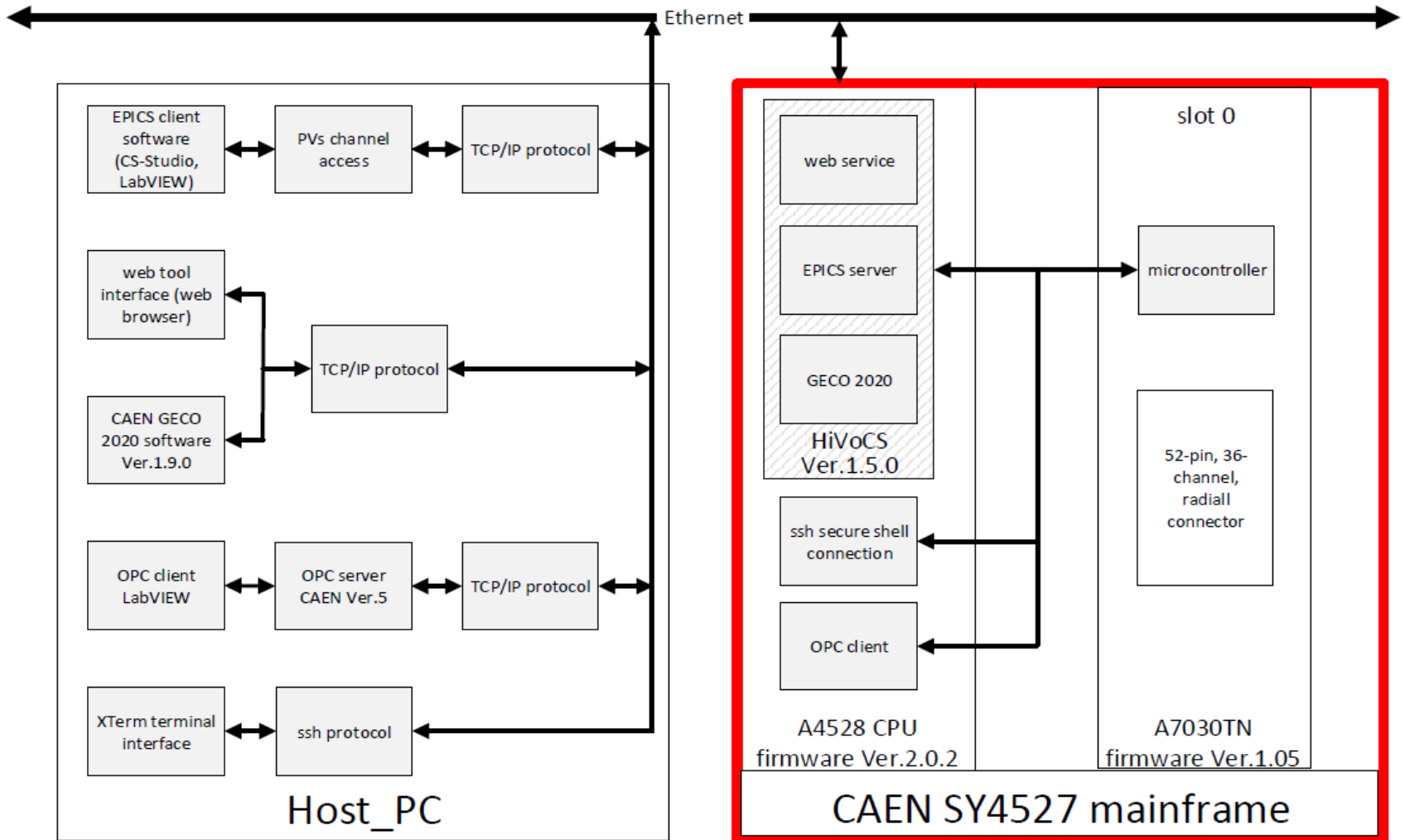
# Hall C: Investigation of CAEN SYS 4527 and HV cards A7030TN



Ramp-up latency

# Hall C: Investigation of CAEN SYS 4527 and HV cards A7030TN

- Test system configuration possibilities



# Thanks Alberto

Dsg-hallc\_controls <dsg-hallc\_controls-bounces@jlab.org>  
on behalf of  
Alberto Lucchesi  
<a.lucchesi@caen.it>  
Fri 9/13/2019 8:25 AM

Dear Pablo,  
thanks to your suggestions we were able to reproduce the same test as described in your document and we found some interesting information...



DSG's inner child

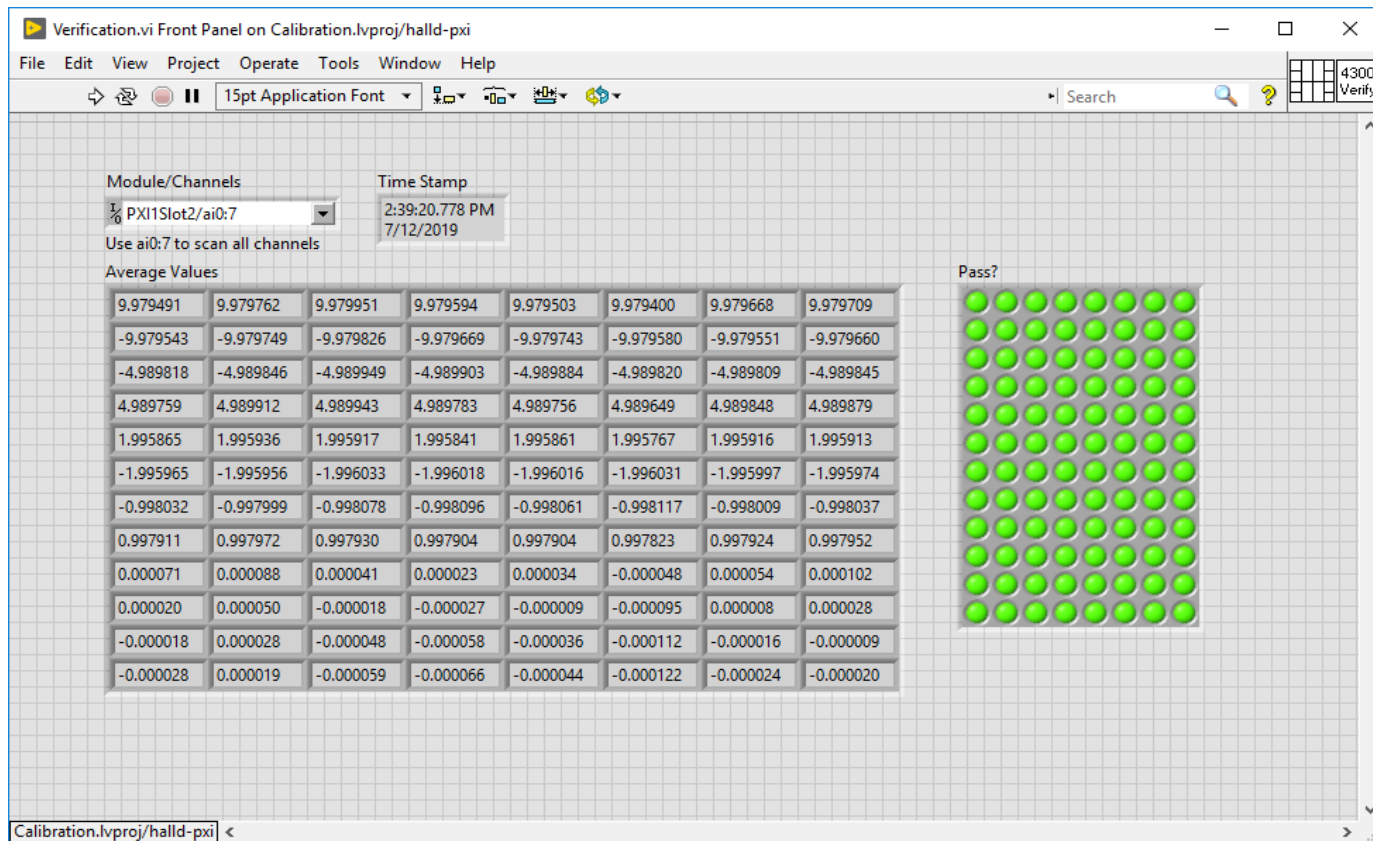
Dsg-hallc\_controls <dsg-hallc\_controls-bounces@jlab.org>  
on behalf of Alberto Lucchesi  
<a.lucchesi@caen.it>  
Mon 9/30/2019 7:26 AM

Dear Pablo,  
from the log I'm convinced that the ramp delay is something related to the board firmware. I say this because looking the log it is clear that all the power on commands are received by the boards at the same time, but for a reason that we have to understand, sometime a channel doesn't perform the ramp correctly but its first 5/6 steps are anomalous...



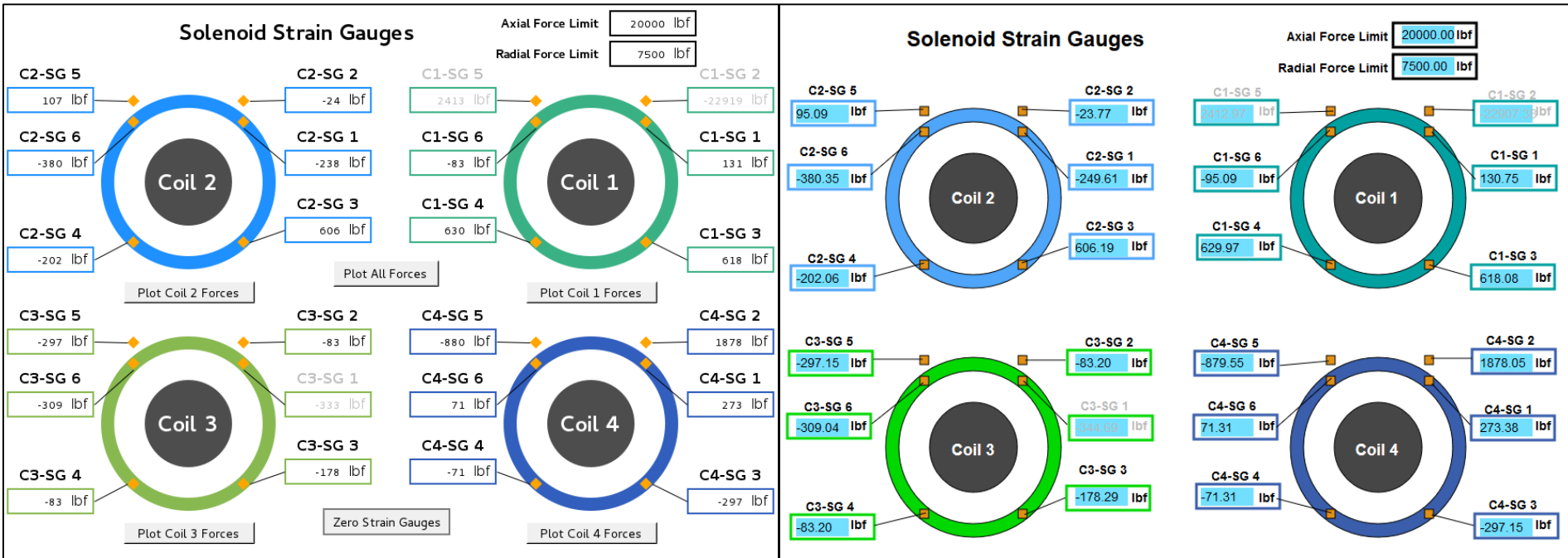
# Hall D: Upgrade of PXI system

- Upgrade and maintenance of PXI system used for FastDAQ (10 kHz to EPICS) of solenoid signals
  - LabVIEW upgraded to 2019, ADC module calibrations performed



# Hall D: WEDM

- 19 CSS screens converted to WEDM for off-site monitoring.



Solenoid Strain Gauges CSS screen

Solenoid Strain Gauges WEDM screen

[DSG Note 2019-51](#), [DSG Talk 2019-19](#)

# Thanks Tim

whitey@jlab.org

Re: [Dsg-halld\_plc] Hall D WEDM status

Dsg-halld\_plc

on behalf of Timothy Whitlatch

Mon 6/24/2019 9:25 AM

Hi Tyler,

**This is a great start.**

ComCal Environment is fine

DIRC Environment is fine

Main Gas System GUI is fine

CDC Gas system not needed

FDC gas system not needed

Gas system solenoid valve monitor not needed

hall temperature is fine

Solenoid Cryo is fine

Solenoid Interlocks is fine

Solenoid strain gauges is fine

Solenoid vacuum is fine

Solenoid voltage taps is fine

Can the Hall camera screens be linked?

Thanks,

Tim

Dsg-halld\_plc

on behalf of Timothy Whitlatch

Mon 7/15/2019 10:30 AM

Hi Tyler,

**This is very nice and very useful!**

Thank you for following through on this.

Tim Whitlatch

Hall D Engineer

Jefferson Lab

757-269-5087

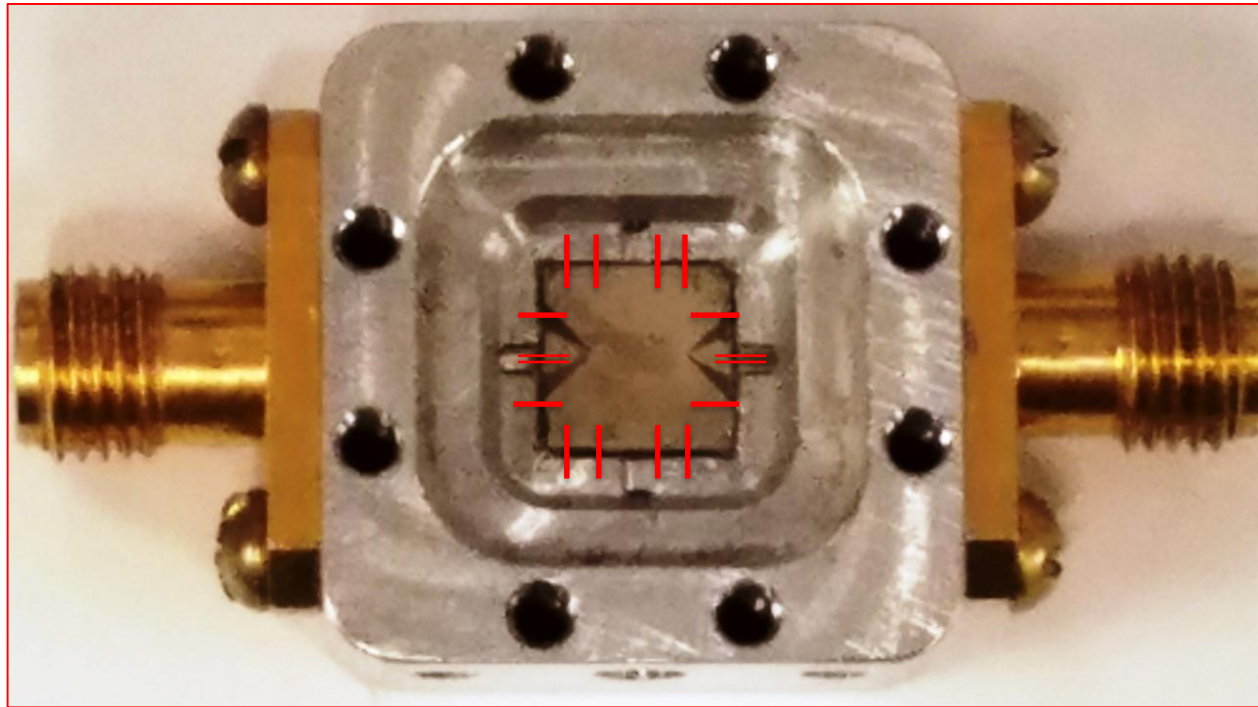


DSG's inner child yet again!

# DSG: Accelerator

- Populating of VME fast shutdown boards for accelerator

[DSG Note 2019-25](#)



- Wirebonding

- Sample made of superconducting Nb<sub>3</sub>Sn, and what is patterned on the surface is a resonator.
- Will be cooling down sample to 4K - 2 K and measure how much energy gets dissipated in heat at a frequency around 2-3GHz. (Junki Makita)



# DSG: R&D and Safety

- NI cRIO Test Station development
  - LabVIEW program to test 18 different types of cRIO modules
  - 18 different types of modules tested

[DSG Note 2019- 17](#), [DSG Note 2019-30](#)

- PLC Test Stand development

[DSG Note 2019- 23](#)

- Prevented three potentially dangerous incidents in EEL
  - “An ounce of prevention ...”

# Thanks Patrizia!

Patrizia Rossi

Thu 10/3/2019 4:45 AM

Dear Marc,  
many thanks for sending out this note to let us know about  
the **commendable behaviour of Mary Ann and Mindy.**

**I am very proud of my group.**

patrizia



# END

- DSG makes crucial and critical contributions to all Halls
- DSG staff well versed with detector hardware and software
  - Controls and Monitoring systems
  - Safety Interlock Systems
  - Detector modelling and detector performance analysis
  - Research and design
- DSG staff
  - Tenacious problem solvers
  - Capable communicators
  - **And most importantly have infectious pleasant personalities**



# Questions?

